In the claims:

Please amend the claims as follows.

1. (original) A memory system comprising a semiconductor memory for storing digital data, said memory being connectable to a control device for receiving an address signal and making available on a output a data selected by means of an address signal,

wherein further comprising a generating circuit for activating of a wait signal to be sent to the control device during reading operations in such a way as to indicate the non availability of the data to be read, and for deactivating the wait signal in such a way as to indicate the availability of the data to be read after a waiting time interval correlated with the actual access time of said memory, this waiting interval having a duration that is variable as a function of the address signal and of at least one operative parameter of said memory system.

2. (original) The system according to claim 1, wherein the generating circuit comprises detection means of address transitions such as to receive the address signal as input and generate a detection signal representative of a modification thereof, the generating circuit being such to activate the wait signal starting from the detection signal.

3. (original) The system according to claim 2, wherein the address signal carries a plurality of address code groups each referring to a hierarchical domain into which the memory is subdivided, and in which said address transition detection means comprise a plurality of transition detection circuits each intended to generate a corresponding transition signal representative of a modification of one of said code groups, the detection signal being obtained by combining the transition signals.

4. (original) The system according to claim 1, wherein the generating circuit comprises circuital means of end-wait signalling for generating an end-wait signal, following said waiting interval, which controls the deactivation of the wait signal.

5. (original) The system according to claim 4, wherein said circuital means of signalling comprise at least one dummy circuit block of such a type as to influence the duration of said waiting interval by an amount that is variable as a function of at least one operative parameter of the memory system and according to a behavior essentially reproducing that associated with at least one architectural and/or structural block of the memory system.

6. (original) The system according to claim 2, wherein the circuital means of end wait signalling are connected to detection means and comprise a plurality of delay networks each associated with a hierarchical domain of the memory, for receiving a corresponding transition signal as input and to generate a corresponding delayed signal, the end wait signal being obtained by a combination of the delayed signals.

7. (original) The system according to claim 6, wherein said plurality of delay networks comprises a first delay network associated with a first hierarchical domain of the memory including a plurality of sub-matrices of the memory, the first delay network being such to introduce into the propagation of the corresponding transition signal which crosses it, a first time delay evaluated on the basis of the actual access time of the memory which occurs following a change in the address signal which implies a change in the sub-matrix within the first hierarchical domain.

8. (original) The system according to claim 7, wherein each delay network of the plurality of delay networks comprises a group of dummy circuit blocks each associated with a corresponding architectural block of the memory

system or structural block of the memory system, each dummy circuit block introducing a second time delay substantially reproducing that introduced by the architectural or structural block to which it is associated.

9. (original) The system according to claim 8, wherein the second time delay of each dummy circuit block is variable as a function of said at least one operative parameter of the memory system and according to a behaviour essentially reproducing that of the corresponding architectural or structural block.

10. (original) The system according to claim 1, wherein said at least one operative parameter comprises a memory supply voltage.

11. (original) The system according to claim 1, wherein said at least one operative parameter comprises the temperature at which the memory system operates.

12. (original) The system according to claim 5, wherein said at least one architectural block is one of the following blocks: an address signal pre-coder, a row decoder, a column decoder, a sense circuit.

13. (original) The system according to claim 5, wherein said at least one structural block is one of the following blocks: a memory row, a memory column, a memory cell.

14. (original) The system according to claim 1, comprising a device for generating a control device timing signal and in which the generating circuit is such to activate and deactivate the wait signal in an asynchronous manner with respect to the timing signal.

15. (original) The system according to claim 1, wherein said memory comprises a flash memory.

16. (original) The system according to claim 1, wherein said memory is arranged according to a plurality of hierarchical domains of the type including memory sectors, rows, columns and words.

17. (original) The system according to claim 8, wherein at least one of said dummy circuit blocks includes one or more electronic components belonging to the structural block or the architectural block to which the dummy circuit block is associated.

18. (Currently amended) A wait circuit for a memory having multiple ~~first and second~~ domains each having a respectively ~~having first and second~~ delay times, the wait circuit, comprising:

an address-transition-detect circuit operable to receive an address signal having multiple ~~first and second~~ sections that respectively correspond to the ~~first and second~~ domains, to detect ~~a~~ respective ~~first~~ signal transitions in the ~~first section and a second signal transition in the second~~ sections, and to generate ~~a~~ respective ~~first~~ transition-detect signals in response to the ~~first~~ signal transitions ~~and a second transition-detect signal in response to the second signal transition~~; and

a delay circuit coupled to the address-transition-detect circuit and operable to transition a wait signal to a wait value in response to the generation of a~~the first or second~~ transition-detect signal~~s and~~ to transition respective delay signals to proceed values the respective delay times or approximately the respective delay times after the generation of the corresponding transition-detect signals, and to transition the wait signal to a proceed value when all of the delay signals have proceed values.~~,~~

~~the first delay time after detection of the first signal transition if no tnsition a first delay signal to a proceed value the first delay time after the generation of the first transition-detect signal, to transition a second delay signal to a proceed value the second delay time after the generation of the second transition-detect~~

~~signal, and to transition the wait signal to a proceed value in response to both of the first and second delay signals having respective proceed values.~~

19.(Canceled).

20. (Canceled).

21. (new) A wait circuit for a memory having multiple domains that each have a respective delay time, the wait circuit comprising:

an address-transition-detect circuit operable to receive an address signal having multiple sections that each correspond to a respective one of the domains and to detect respective signal transitions in at least two of the sections; and

a delay circuit coupled to the address-transition-detect circuit and operable to transition a wait signal to a wait value in response to a detected signal transition and to transition the wait signal to a proceed value after or approximately after the longest one of the delay times that correspond to the detected transitions.

22. (new) The wait circuit of claim 21 wherein the delay circuit:

comprises dummy circuits that are each operable to transition a respective delay signal to a proceed value after or approximately after the delay time of a corresponding domain; and

is operable to transition the wait signal to the proceed value when all of the delay signals have respective proceed values.

23. (new) A method, comprising:

accessing a memory by transitioning bits in multiple sections of an address signal, the sections respectively corresponding to domains of the memory, the domains having respective access delays; and

preventing subsequent access to the memory for or approximately for the longest of the access delays.

24. (new) The method of claim 23 wherein the access delays are dependent on supply voltage.

25. (new) The method of claim 23 wherein the access delays are dependent on temperature.

26. (new) The method of claim 23 wherein preventing subsequent access to the memory comprises:

transitioning multiple delay signals to respective wait values in response to the transitioning of bits in the sections of the address signal, each delay signal corresponding to a respective one of the sections;

transitioning each of the delay signals to a respective proceed value after or approximately after the delay time of a domain that corresponds to the same section of the address signal as the delay signal; and

allowing subsequent access to the memory when all of the delay signals have proceed values.

27. (new) A memory, comprising:

address domains that each have a respective delay time; and

a wait circuit operable to,

receive an address signal having multiple sections that each correspond to a respective one of the domains,

detect respective signal transitions in at least two of the sections,

transition a wait signal to a wait value in response to a detected signal transition, and

transition the wait signal to a proceed value after or approximately after the longest one of the delay times that correspond to the detected transitions.

28. (new) The memory of claim 27, further comprising a pre-decode circuit coupled to the wait circuit and operable to generate the address signal from a raw address signal.

29. (new) A data circuit, comprising:

a memory controller operable to receive a wait signal and to transition a raw address signal when the wait signal has proceed value; and

a memory coupled to the memory controller and operable to generate the wait signal, the memory comprising,

address domains that each have a respective delay time,

a decode circuit operable to convert the raw address signal into a decoded address signal having sections that each correspond to a respective one of the domains, and

a wait circuit coupled to the decode circuit and operable to,

detect respective signal transitions in at least two of the sections of the decoded address signal,

transition the wait signal to a wait value in response to a detected signal transition, and

transition the wait signal to the proceed value after or approximately after the longest one of the delay times that correspond to the detected transitions.

30. (new) An electronic system, comprising:

a data circuit, comprising,

a memory controller operable to receive a wait signal and to transition a raw address signal when the wait signal has proceed value, and

a memory coupled to the memory controller and operable to generate the wait signal, the memory comprising,

address domains that each have a respective delay time,

a decode circuit operable to convert the raw address signal into a decoded address signal having sections that each correspond to a respective one of the domains, and

a wait circuit coupled to the decode circuit and operable to,

detect respective signal transitions in at least two of the sections of the decoded address signal,

transition the wait signal to a wait value in response to a detected signal transition, and

transition the wait signal to the proceed value after or approximately after the longest one of the delay times that correspond to the detected transitions.